

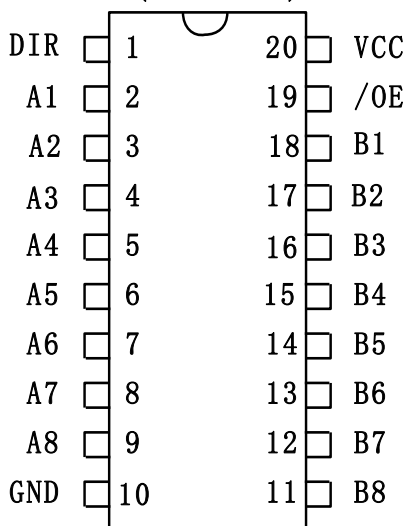


**74HC245**(文件编号: S&CIC0524)

### OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- High-current 3-stage outputs drive bus lines directly or up to 15 LSTTL loads
- Package options include plastic small-outline (DW), shrink small-outline (DB), thin shrink small-outline (PW), and ceramic flat (W) packages, ceramic chip carriers (FK), and standard plastic (N) and ceramic (J) 300-mil DIPs

74HC245... D, DB, N, OR PW PACKAGI  
(TOP VIEW)



### DESCRIPTION

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (/OE) input can be used to disable the device so that the buses are effectively isolated.

The 74HC245 is characterized for operation from -40°C to 85°C.

**FUNCTION TABLE**  
(each gate)

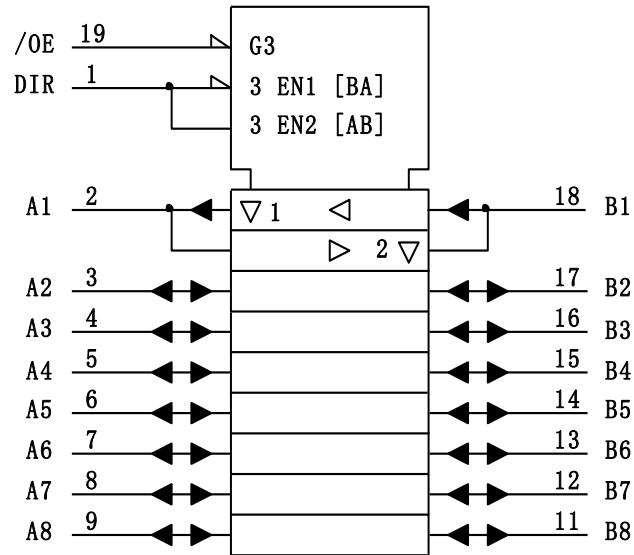
INPUTS		OUTPUT
/OE	DIR	Y
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



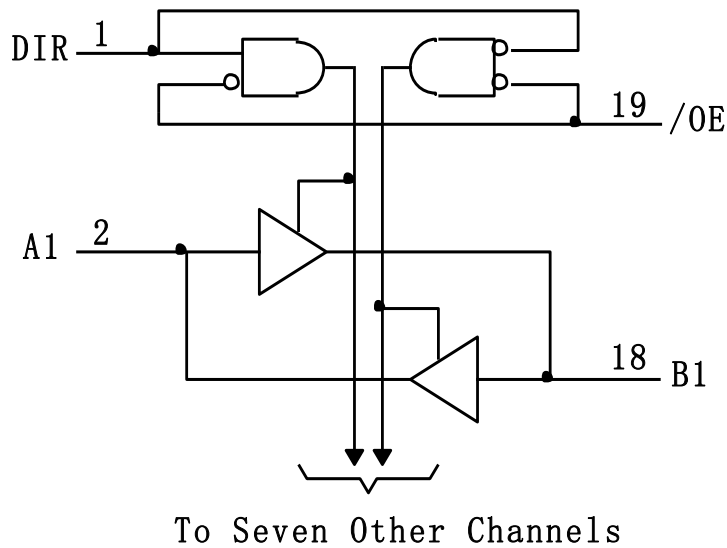
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## OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

### LOGIC SYMBOL



### LOGIC DIAGRAM (positive logic)







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### OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		Vcc	T <sub>A</sub> = 25°C			74HC245		UNIT
				MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20uA	2V	1.9	1.998	-	1.9	-	V
			4.5V	4.4	4.499	-	4.4	-	
			6V	5.9	5.999	-	5.9	-	
		I <sub>OH</sub> = -6mA	4.5V	3.98	4.3	-	3.84	-	
		I <sub>OH</sub> = -7.8mA	6V	5.48	5.8	-	5.34	-	
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = 20uA	2V	-	0.002	0.1	-	0.1	V
			4.5V	-	0.001	0.1	-	0.1	
			6V	-	0.001	0.1	-	0.1	
		I <sub>OH</sub> = 6mA	4.5V	-	0.17	0.26	-	0.33	
		I <sub>OH</sub> = 7.8mA	6V	-	0.15	0.26	-	0.33	
I <sub>I</sub>	DIR or /OE	V <sub>I</sub> = Vcc or 0	6V	-	±0.1	±100	-	±1000	nA
I <sub>OZ</sub>	A or B	V <sub>O</sub> = Vcc or 0	6V	-	±0.01	±0.5	-	±5	uA
I <sub>cc</sub>		V <sub>I</sub> = Vcc or 0, I <sub>O</sub> = 0	6V	-	-	8	-	80	uA
C <sub>i</sub>	DIR or /OE		2V to 6V	-	3	10	-	10	pF

Switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC	T <sub>A</sub> = 25°C			74HC245		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	2V	-	40	105	-	130	ns
			4.5V	-	15	21	-	26	
			6V	-	12	18	-	22	
t <sub>en</sub>	/OE	A or B	2V	-	125	230	-	290	ns
			4.5V	-	23	46	-	58	
			6V	-	20	39	-	49	
t <sub>dis</sub>	/OE	A or B	2V	-	74	200	-	250	ns
			4.5V	-	25	40	-	50	
			6V	-	21	34	-	43	
t <sub>t</sub>		A or B	2V	-	20	60	-	75	ns
			4.5V	-	8	12	-	15	
			6V	-	6	10	-	13	



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**OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

Switching characteristics over recommended operating free-air temperature range,  $C_L = 150\text{pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC	$T_A = 25^\circ\text{C}$			74HC245		UNIT
				MIN	TYP	MAX	MIN	MAX	
tpd	A or B	B or A	2V	-	54	135	-	170	ns
			4.5V	-	18	27	-	34	
			6V	-	15	23	-	29	
t <sub>en</sub>	/OE	A or B	2V	-	150	270	-	335	ns
			4.5V	-	31	54	-	37	
			6V	-	25	46	-	56	
t <sub>t</sub>		A or B	2V	-	45	210	-	265	ns
			4.5V	-	17	42	-	53	
			6V	-	13	36	-	45	

Operating characteristics,  $T_A = 25^\circ\text{C}$

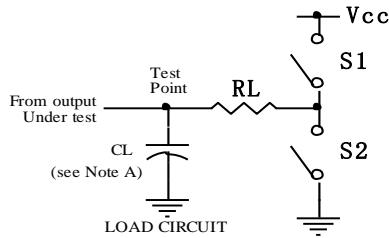
PARAMETER	TEST CONDITIONS	TYP	UNIT
Cpd power dissipation capacitance per gate	No load	40	pF



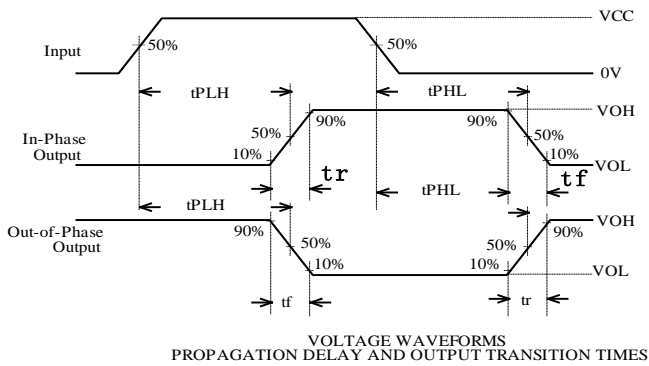
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OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

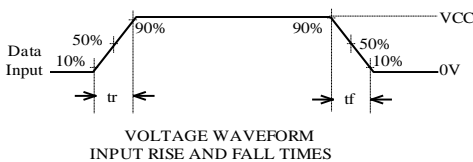
PARAMETER MEASUREMENT INFORMATION



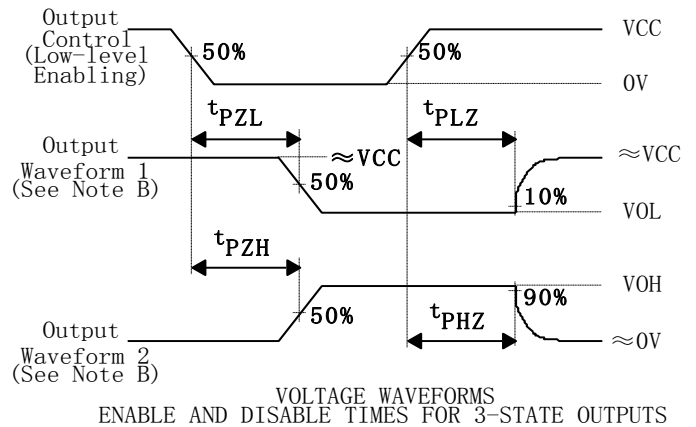
PARAMETER	RL	CL	S1	S2
$t_{en}$	1K $\Omega$	50pF or 150pF	Open	Closed
			Closed	Open
$t_{dis}$	1K $\Omega$	50pF	Open	Closed
			Closed	Open
$t_{pd}$ or $t_t$	—	50pF or 150pF	Open	Open



VOLTAGE WAVEFORMS PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A.  $C_L$  includes probe and test-fixture capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.

D. The outputs are measured one at a time with one input transition per measurement.

E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load circuit and voltage waveforms