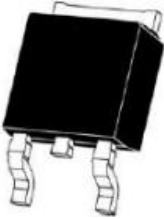

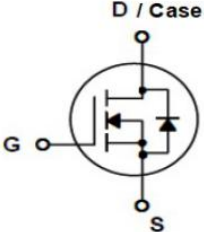




Description

<p>Product Summary</p> <ul style="list-style-type: none"> • VDS 30V • ID 80A • RDS(ON)(at VGS=10V) <5.5 mohm • RDS(ON)(at VGS=4.5V) <8.0 mohm • 100% UIS Tested • 100% ∇VDS Tested 	<p>General Description</p> <ul style="list-style-type: none"> • Trench Power LV MOSFET technology • Excellent package for heat dissipation • High density cell design for low RDS(ON) <p>Applications</p> <ul style="list-style-type: none"> • High current load applications • Load switching • Hard switched and high frequency circuits • Uninterruptible power supply
<p>Package</p> <div style="display: flex; justify-content: space-around; align-items: center;">    </div> <p style="text-align: center;">TO-252</p>	

Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter		Limit	Unit
VDS	Drain-source Voltage		30	V
VGS	Gate-source Voltage		±20	V
ID	Drain Current	TC=25°C	80	A
		TC=100°C	51	
IDM	Pulsed Drain Current A		190	A
PD	Total Power Dissipation	TC=25°C	45	W
		TC=100°C	22.5	W
EAS	Single Pulse Avalanche Energy B		205	mJ
RθJC	Thermal Resistance Junction-to-Case C		3.0	°C/W
TJ ,TSTG	Junction and Storage Temperature Range		-55~+175	°C



Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Static Parameter						
BVDSS	Drain-Source Breakdown Voltage	VGS= 0V, ID=250μA	30			V
IDSS	Zero Gate Voltage Drain Current	VDS=30V, VGS=0V			1	μA
IGSS	Gate-Body Leakage Current	VGS= ±20V, VDS=0V			±100	nA
VGS(th)	Gate Threshold Voltage	VDS= VGS, ID=250μA	1.0	1.5	2.5	V
RDS(ON)	Static Drain-Source On-Resistance	VGS= 10V, ID=20A		3.8	5.5	mΩ
		VGS= 4.5V, ID=15A		6.2	8.0	
VSD	Diode Forward Voltage	IS=20A, VGS=0V		0.80	1.2	V
IS	Maximum Body-Diode Continuous Current				80	A
Dynamic Parameters						
Ciss	Input Capacitance	VDS=15V, VGS=0V, f=1MHZ		2150		pF
Coss	Output Capacitance			435		
Crss	Reverse Transfer Capacitance			252		
Switching Parameters						
Qg	Total Gate Charge	VGS=10V, VDS=15V, ID=20A		52.8		nC
Qgs	Gate-Source Charge			12.3		
Qgd	Gate-Drain Charge			10.8		
Qrr	Reverse Recovery Charge	IF=20A, di/dt=100A/us		28		
trr	Reverse Recovery Time			27		
tD(on)	Turn-on Delay Time	VGS=10V, VDD=20V, ID=2A, RL=1Ω RGEN=3Ω		9		ns
tr	Turn-on Rise Time			15.5		
tD(off)	Turn-off Delay Time			29		
tf	Turn-off fall Time			9		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. T_J=25°C, V_{DS}=30V V_{DD}=15V V_{GS}=10V L=0.5mH.

C. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



Typical Performance Characteristics

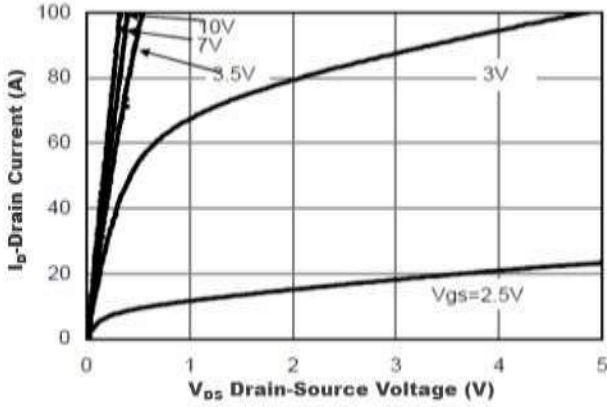


Figure1. Output Characteristics

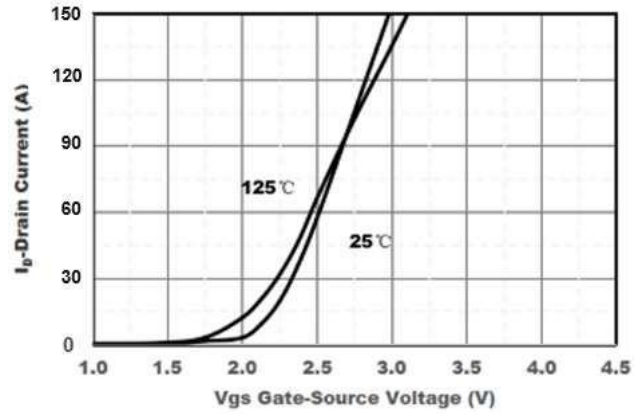


Figure2. Transfer Characteristics

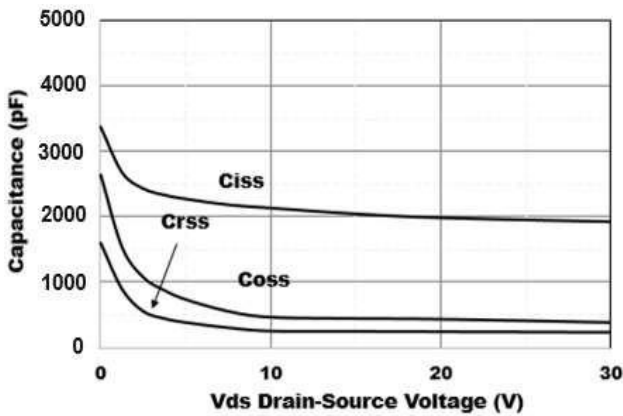


Figure3. Capacitance Characteristics

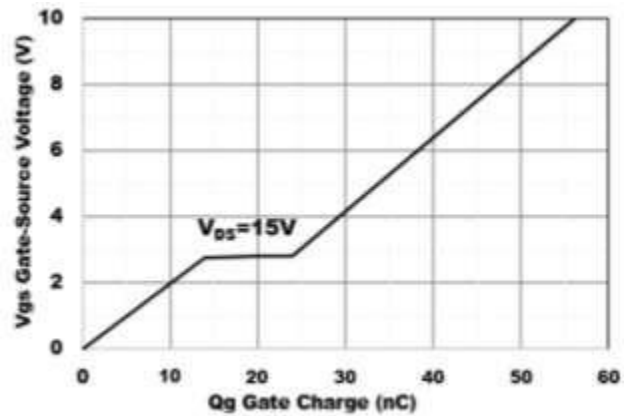


Figure4. Gate Charge

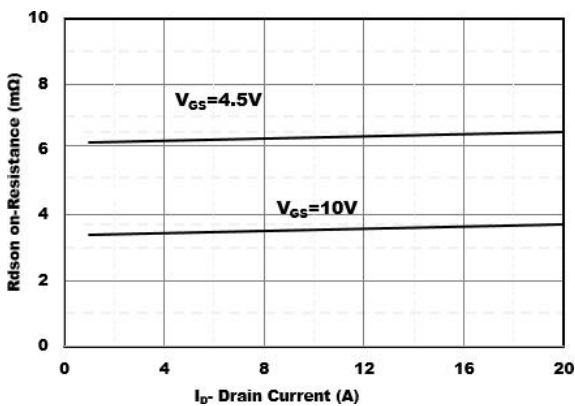


Figure5. Drain-Source on Resistance

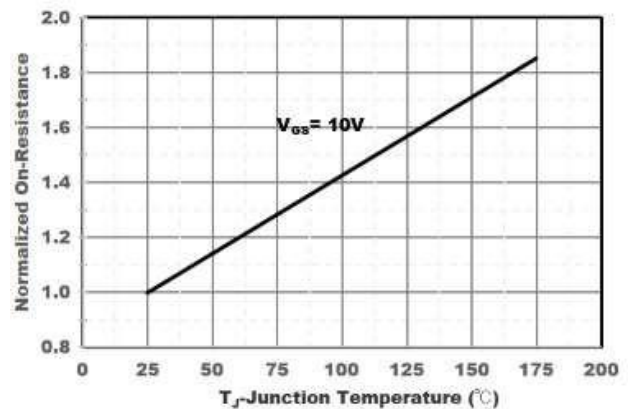


Figure6. Drain-Source on Resistance

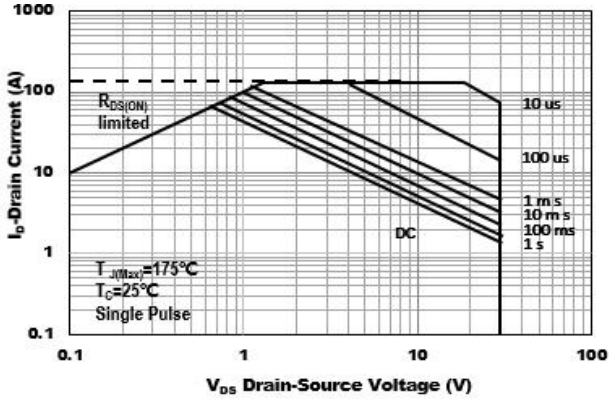


Figure7. Safe Operation Area

Test Circuit

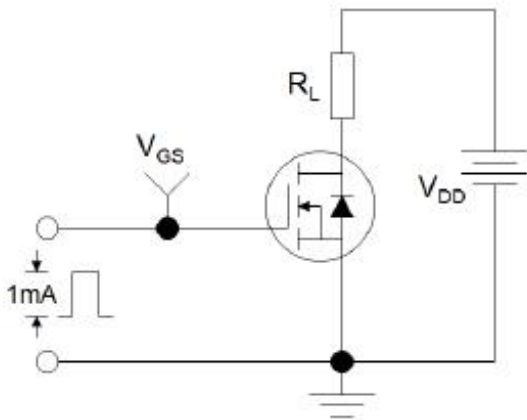


Figure1:Gate Charge Test Circuit & Waveform

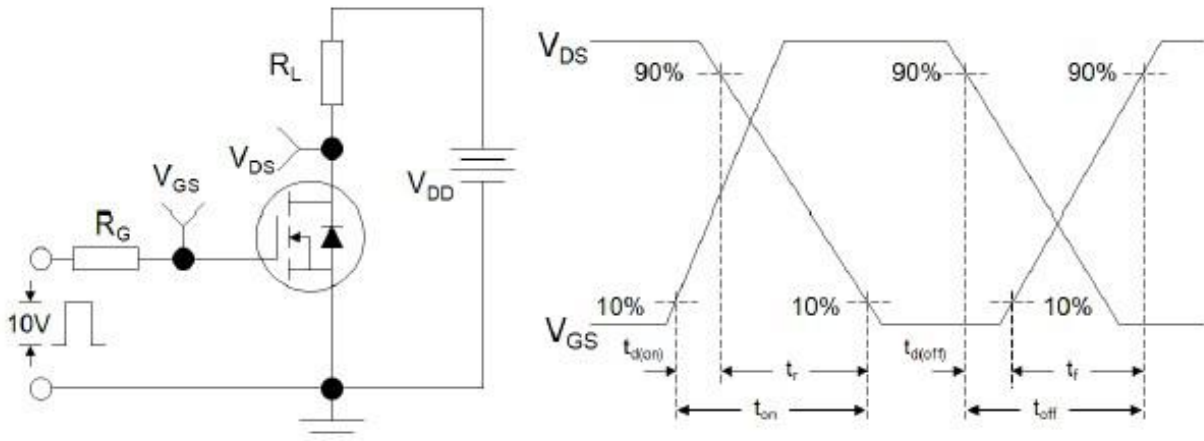


Figure 2: Resistive Switching Test Circuit & Waveforms

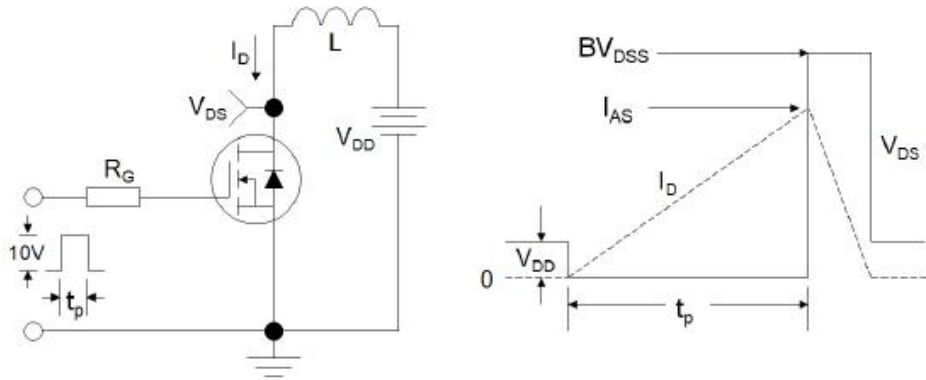
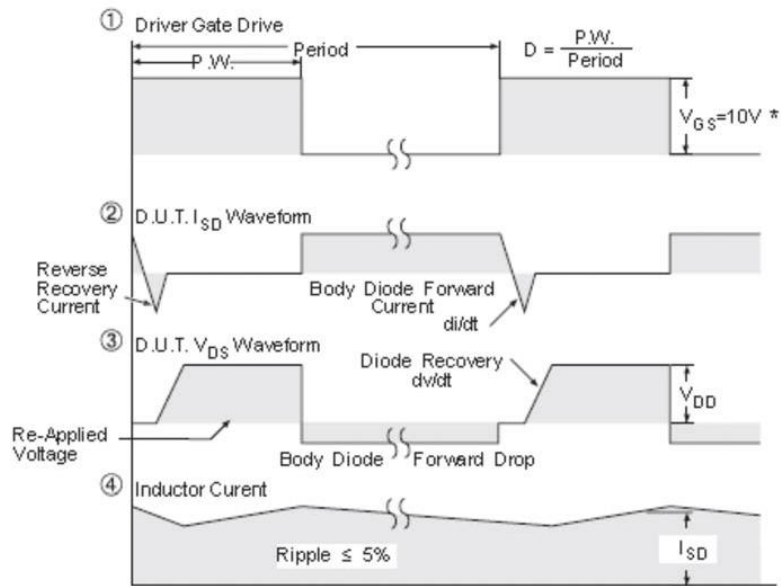
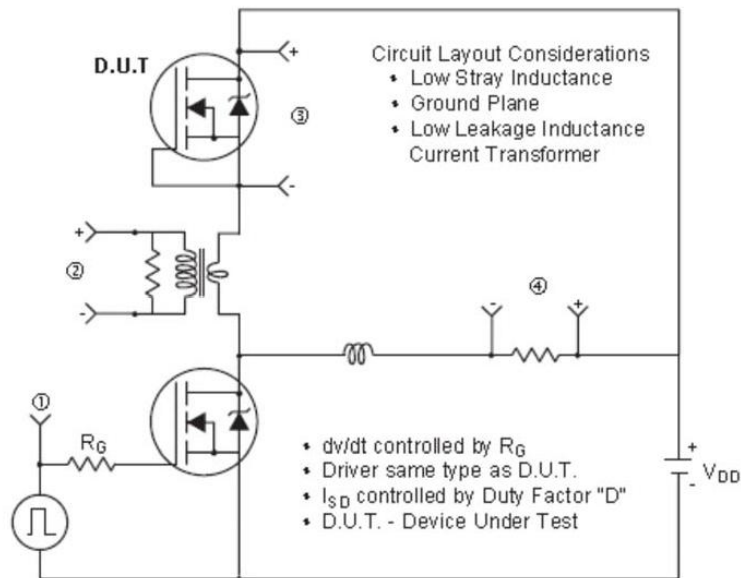


Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms

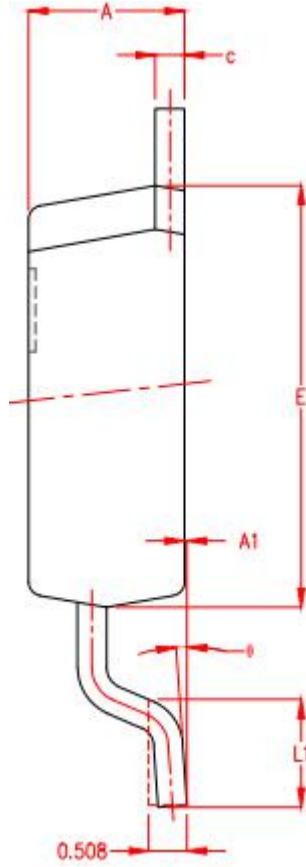
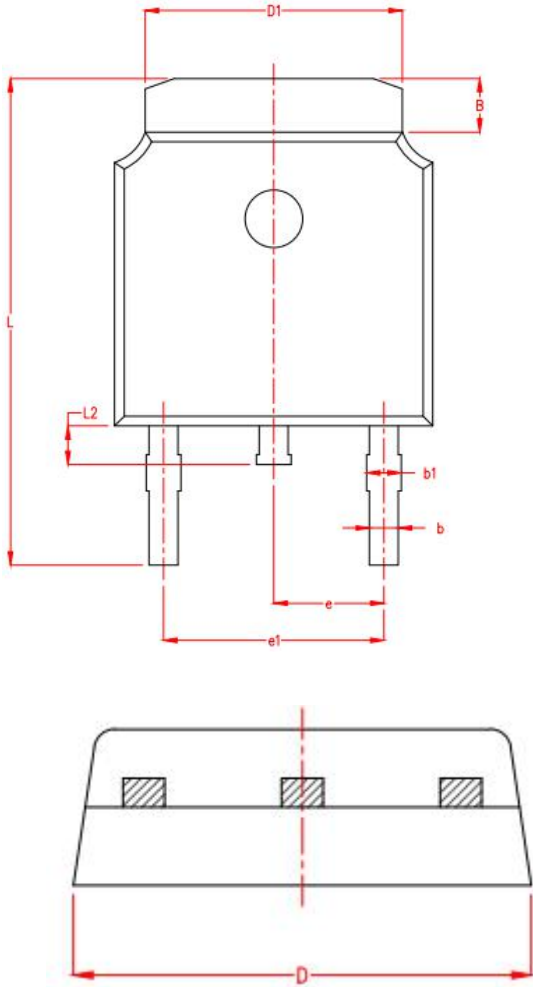


* $V_{GS} = 5V$ for Logic Level Devices

Figure 4: Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)



TO-252 Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.15	2.25	2.35
A1	0.00	0.06	0.12
B	0.96	1.11	1.26
b	0.59	0.69	0.79
b1	0.69	0.81	0.93
c	0.34	0.42	0.50
D	6.45	6.60	6.75
D1	5.23	5.33	5.43
E	5.95	6.10	6.25
e	2.286TYP.		
e1	4.47	4.57	4.67
L	9.90	10.10	10.30
L1	1.40	1.55	1.70
L2	0.60	0.80	1.00
θ	0°	4°	8°