



## DESCRIPTION

SC8211 is a dual channel, 16 bit digital -to-analog converter IC utilizing CMOS technology specially designed for the digital audio applications. The internal conversion architecture is based on a R-2R resistor ladder network, internal circuit is well matched and a 16 bit dynamic range is achieved even in whole supply voltage range. SC8211 also enhanced the performance of timing responsibility in digital serial bus, in a company with the fast switching R-2R network that make 8X over sampling audio signal is also supported.

SC8211 can be supported wide range of sample frequency, it is compatible with TDA1311 by functionally. It's digital input timing format is Least Significant Bit Justified (LSBJ), or so called Japanese input format. Digital code format is two's complement and MSB first. SC8211 is available in 8-pin SOP or DIP.

## FEATURES

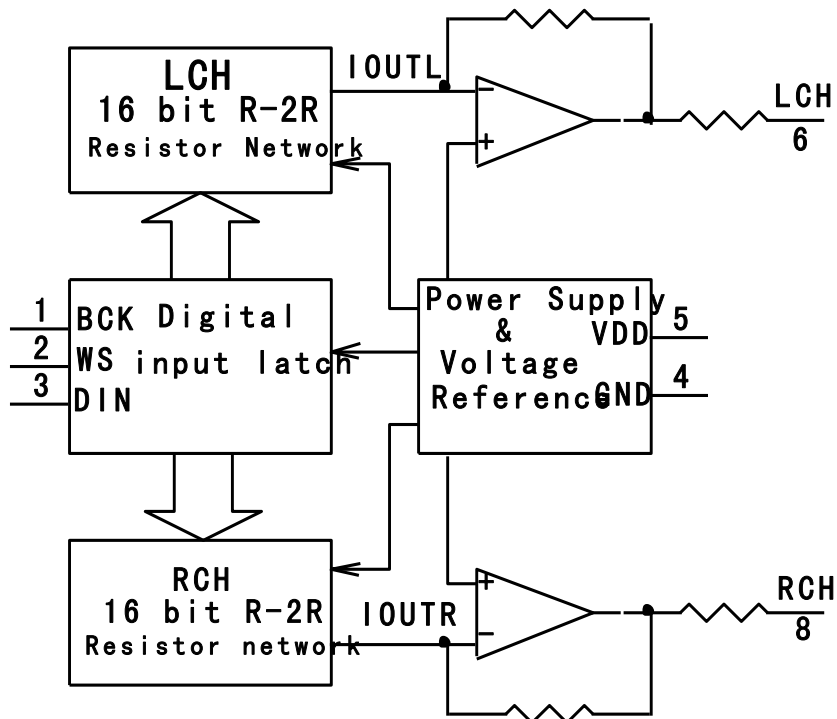
- CMOS technology
- Support 3.3V bus input level
- Low power consumption
- Two audio channel output in the same chip
- 16 bit dynamic range
- Low total harmonic distortion
- No phase shift between both output channel
- Available in 8 pins, SOP or DIP

## APPLICATIONS

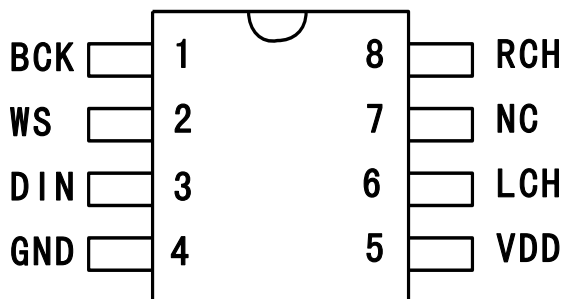
- Digital audio equipment
- CD ROM/VCD
- Multimedia sound card
- MPEG decoder card



**BLOCK DIAGRAM**



**PIN CONFIGURATION**



**PIN DESCRIPTION**

Pin Name	I/O	Description	Pin No.
BCK	I	Serial bit clock input	1
WS	I	Word select clock input pin	2
DIN	I	Data input pin	3
GND	-	Ground	4
VDD	Power	Positive power supply	5
LCH	O	Left channel output	6
NC	-	No connection	7
RCH	O	Right channel output	8



## FUNCTION DESCRIPTION

The serial bus input data format of SC8211 is Japanese or called LSBJ (Least significant bit justified) format. Each valid DIN data will be shifted to the input register in the rising edge of the BCK, only the first 16 bit data (from MSB) is valid if the input data length is more than 16 bit, other data bit will be truncated. The clock frequency of the BCK could run up to 20MHz and supported to 8X over-sampling in 48KHz WS clock rate. Both left and right data words are time multiplexed. Please refer to the diagrams for timing and input signal formats.

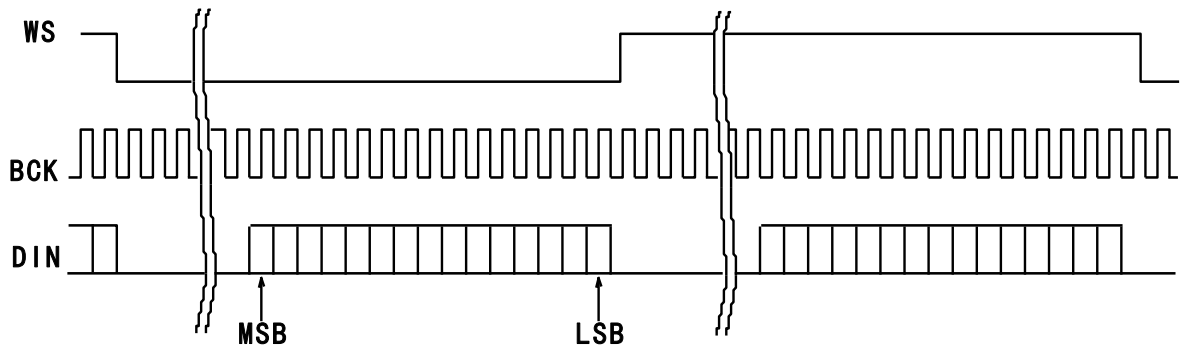
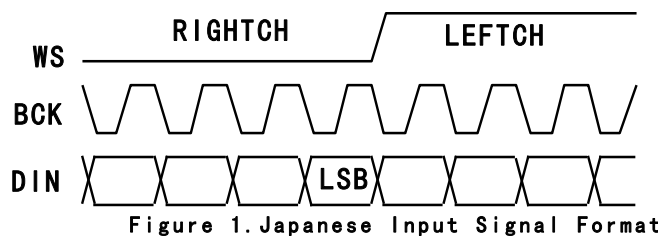


Figure 2. Timing and Input Signal Formats

The DIN data must be the 2's complementary format and the MSB (Most significant bit) must be the first. When the word select (WS) clock in the Low level, the DIN data will be shifted to the right input register. Likewise, the DIN data will be shifted to the left input register when WS clock in the high level. The buffered DIN data then feeding to the DAC after both input register are all settled down, this can eliminated the phase shift happened between two channel output. DAC output is generated by a 16 bit R-2R resistor ladder network. This signal is driven to the Right/ Left Channel (RCH/LCH) via the buffer operational amplifier.

## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power supply voltage	$V_{DD}$	-0.3~7.0	V
Input voltage	$V_I$	-0.3~ $V_{DD}+0.3$	V
Operating temperature	$T_{opr}$	-40~+85	°C
Storage temperature	$T_{stg}$	-65~+150	°C



**DC CHARACTERISTICS**(Test conditions: Ta = 25°C, VDD = 5.0V, unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power supply voltage	VDD	THD<1%	3	5	6	V
Operating current	Is	VDD=5V	10	13	18	mA
Digital input high level*1	V <sub>IH</sub>		1.8	2.2	VCC	V
Digital input low level*1	V <sub>IL</sub>		GND	1.2	1.8	V

Note: \*1 digital input level will changed due to supply voltage.

**TIMING CHARACTERISTICS** (Please to the figure 1)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Bit clock frequency	F <sub>bck</sub>	BCK	-	-	18.4	MHz
Word clock frequency	F <sub>ws</sub>	WS	-	-	384	KHz
Input data rate	F <sub>din</sub>	DIN	-	-	18.4	Mbits/S
H level time	t <sub>H</sub>		25			ns
Rise time	t <sub>R</sub>				20	ns
Fall time	t <sub>F</sub>				20	ns

**ANALOG AUDIO CHARACTERISTICS**

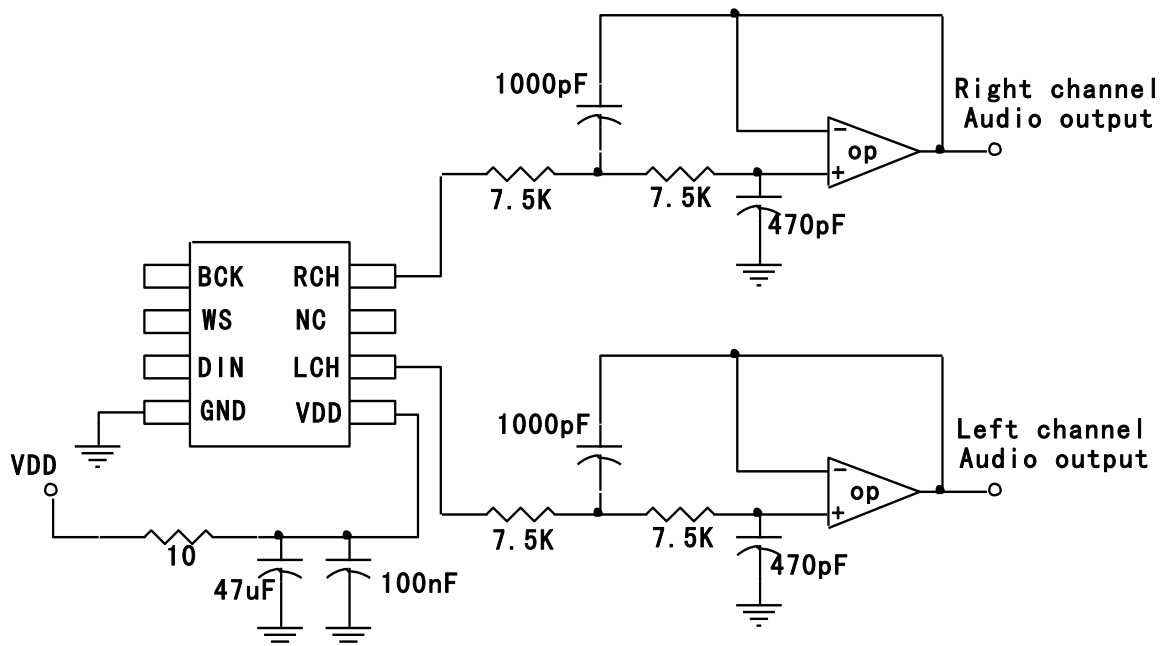
(Test condition: Ta = 25°C, VDD = 5.0V, unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Maximum output level	VO		2.2	2.5	2.7	VPP
Total harmonic distortion	THD	1KHz, 0dB Fs	-	0.13	0.3	%
		1KHz, -10dB Fs	0.08	0.1	0.2	
		1KHz, -60dB Fs	-	3	6	
Monotonicity	Mt		-	-	16	Bit
Dynamic range	DR		85	89	-	dB
Signal to noise ratio	S/N	Data = 0000H	89	93	-	dB
		No clock input	-	95	97	
Cross talk	C <sub>ta</sub>	Both output Channel	80	89	92	dB
	C <sub>Td</sub>	Digital in to Analog out	75	80	-	
Phase shift	Pd	Both output channel	-	0	0.2	uS



### APPLICATION CIRCUIT AND NOTE

To further suppress residual noise, we suggest placing an additional low pass filter after the analog output of SC8211. Please refer to the circuit diagram below. This is a simple second-order analog post filter. If low noise output is very important for your circuit design we suggest using a regulated power supply.



### ORDERING INFORMATION

Order part number	Package type	Top code
SC8211-S	8 Pins, SOP, 150mil	SC8211-S
SC8211	8 Pins, DIP, 300mil	SC8211

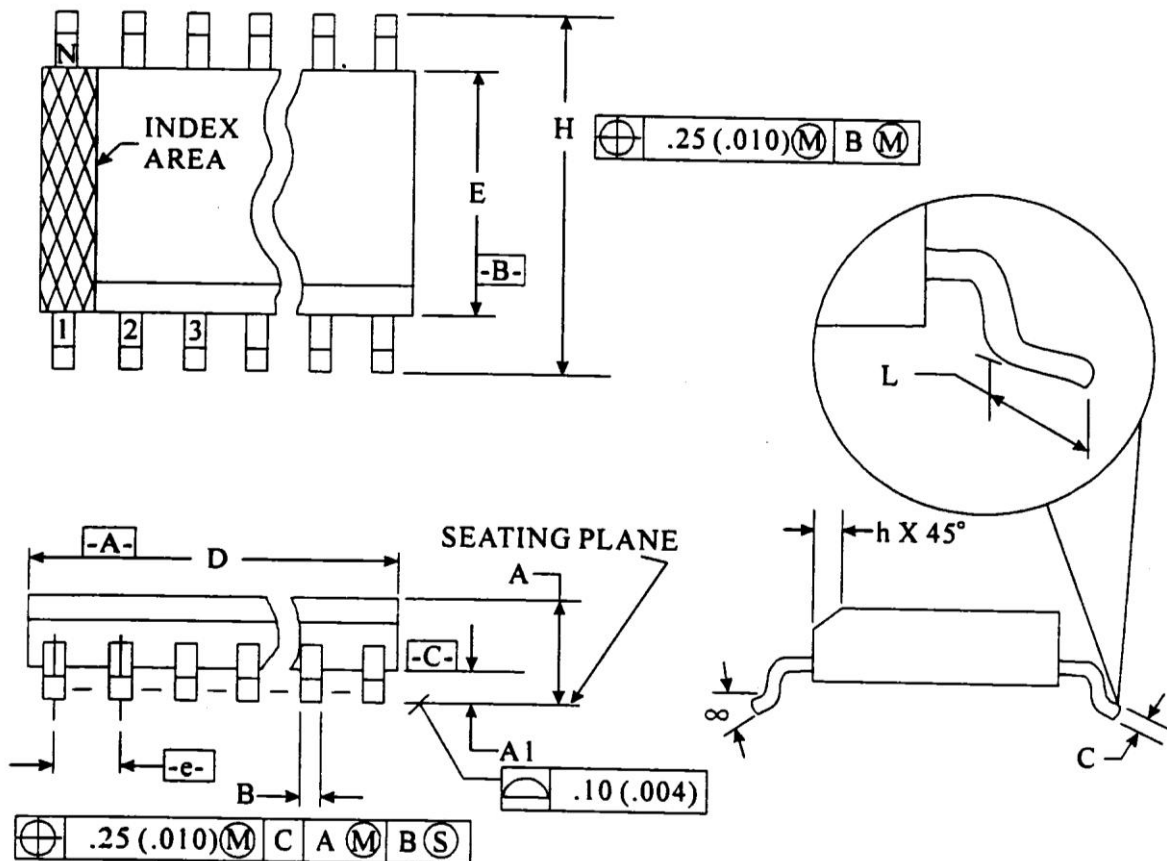
Notes:

1. (L) = Lead Free
2. The lead free mark is put in front of the date code.



## PACKAGE INFORMATION

8 PINS, SOP, 1500MIL



Symbol	Min	Nom	Max
A	1.35		1.75
A1	0.10		0.25
B	0.33		0.51
C	0.19		0.25
D	4.80		5.00
E	3.80		4.00
E		1.27 bsc.	
H	5.80		6.20
H	0.25		0.50
L	0.40		1.27
$\alpha$	0°		8°



Notes:

1. Dimensioning and tolerance per ANSI Y14.5M-1982.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension "E" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. "L" is the length of the terminal for soldering to a substrate.
6. N is the number of the terminal positions (N = 8).
7. The lead width "B" as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in).
8. Controlling dimension: MILLIMETER.
9. Refer to JEDEC MS-0.12, Variation AA.

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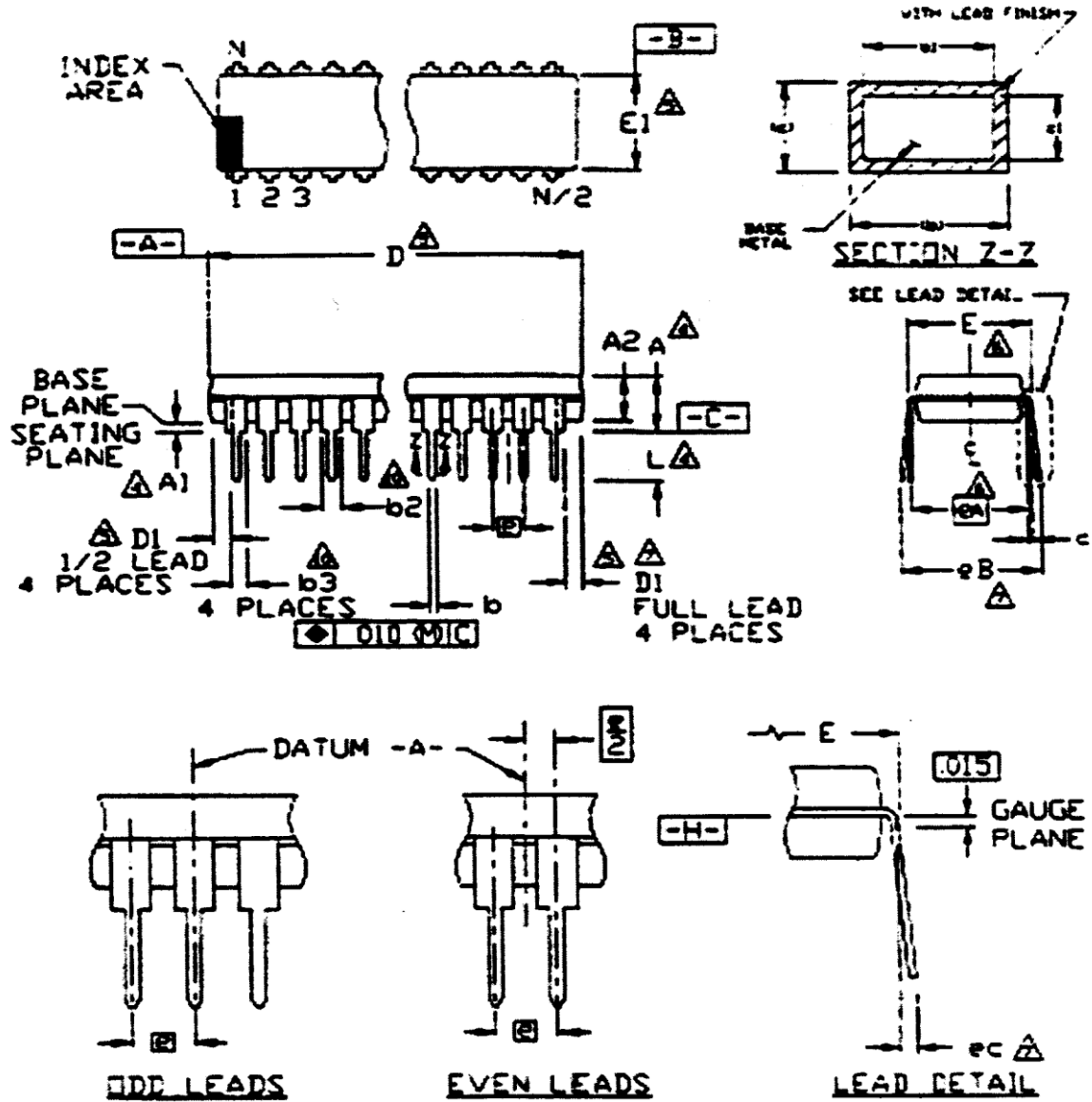
# 深圳市富满电子有限公司

SHENZHEN FUMAN ELECTRONICS CO., LTD.

SC8211(文件编号: S&CIC0452)

16 Bit Digital to Analog Converter

8PINS, DIP, 300MIL







Symbol	Min	Nom	Max
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.355	0.365	0.400
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	0.100 bsc.		
eA	0.300 bsc.		
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes:

- Controlling dimensions: INCHES.
- Dimensioning and tolerance per ANSI Y14.5M-1982.
- Symbols are defined in the “MO Series Symbol LIST” in section 2.2 of publication No.95.
- Dimension A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1 and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
- E and eA measured with the leads constrained to be perpendicular to data -c-.
- eB and eC are measured at the lead tips with the leads unconstrained.
- N is the number of leads (N = 8).
- Pointed or rounded lead tips are preferred to ease insertion.
- b2 and b3 maximum dimensions do not include dam bar protrusions. Dam bar protrusions shall not exceed 0.010 inch (0.25mm).
- Variation BA has a b3 dimension and is 1/2 lead package.
- Distance between the leads including dam bar protrusions to be 0.005 inch minimum.
- Datum plane -H- coincident with the bottom of lead, where lead exits the body.
- Refer to JEDEC MS-001, Variation BA.

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